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APPENDIX 31
AUXILIARY BUS INTERFACE
FINAL SOFTWARE REPORT
DATA ITEM NO. A005

INTEGRATED ELECTRONIC WARFARE SYSTEM
ADVANCED DEVELOPMENT MODEL (ADM)

PREPARED FOR
NAVAL AIR DEVELOPMENT CENTER
WARMINSTER, PENNSYLVANIA

CONTRACT N62269-75-C-0070

RAYTHEON
ELECTROMAGNETIC
SYSTEMS DIVISION

1 OCTOBER 1977

APPENDIX 31
AUXILIARY BUS INTERFACE

FINAL SOFTWARE REPORT

DATA ITEM A005

INTEGRATED ELECTRONIC WARFARE SYSTEM (IEWS)
ADVANCED DEVELOPMENT MODEL (ADM)

Contract No. N62269-75-C-0070

Prepared for:

Naval Air Development Center
Warminister, Pennsylvania

Prepared by:

RAYTHEON COMPANY
Electromagnetic Systems Division
6380 Hollister Avenue
Goleta, California 93017

1 OCTOBER 1977

RAYTHEON	RAYTHEON COMPANY LEXINGTON, MASS. 02173	CODE IDENT NO. 49956	SPEC NO. 53959-JK-1003	
			SHEET 1 OF 14	REV 2

TYPE OF SPEC

INTERFACE CONTROL DOCUMENT

TITLE OF SPEC

AUXILIARY BUS ICD

FUNCTION	APPROVED	DATE	FUNCTION	APPROVED	DATE
WRITER	J. Kolanek	25 July 1975			

REVISIONS

CHK	DESCRIPTION	REV	CHK	DESCRIPTION	REV
CPF JCM	Complete Revision 12/15/75	1			
CRD	See Below 8/5/76	2			

Title:
Was: SORTER AUXILIARY OUTPUT ICD
IS: AUXILIARY BUS ICD

Para. 3.1.3
Was: ... Equipment shall respond by raising...
Is: Equipment shall respond by lowering...

Figure 3: 2 places
Was: USFG
Is: UPDW
Was: Technique Number
Is: ET Channel Number
Was: 0 = Unassoc. PDW
Is: 1 = Unassoc. PDW

Was: Tech. Gen. Only
Is: To Tech. Gen. & Emitter Tracker
Was: 1 = Tech. Gen. Destin.
Is: AGTG · $\overline{\text{UPDW}}$ = Tech. Gen. or Emitter Tracker Destin.
Was: 1 = Sys. Contr. Destin
Is: SC V UPDW = Sys. Contr. Destin.

Figure 5.
Add: pin numbers

REVISION																								
SHEET NO.																								
REV STATUS OF SHEETS	REVISION																							
	SHEET NO.																							

1.0 SCOPE

This document shall specify the auxiliary output from Sorter. The functional as well as detailed physical requirements shall be included in this specification.

2.0 APPLICABLE DOCUMENTS

(TBD).

3.0 REQUIREMENTS

3.1 INTERFACE DEFINITION

3.1.1 General

An interface shall be defined at the Sorter which provides Jammer Pulse Words (JPW), Unassociated Pulse Descriptor Words (UPDW) and/or Selected Pulse Descriptor Words (SPDW). A number of users shall simultaneously have access to this interface and shall at least include: Emitter Tracker, Technique Generator, System Controller and the Special Test Equipment.

The interconnections among the various units shall be organized functionally as shown in Figure 1. Units shall be interconnected using a synchronous bus structure which allows either the Sorter or the Special Test Equipment to output data on the bus. All other units shall be destination devices. In addition, the Special Test Equipment shall monitor the data traffic generated by the Sorter.

3.1.2 Bus Structure

The interface shall consist of three sets of lines.

a. 16 DATA lines

b. 4 IDENT lines

c. 3 control lines LOAD, $\overline{\text{ACTIVE}}$, ENABLE

The DATA lines shall be used to transfer the output message contents. The IDENT lines shall be used to identify the content of the DATA. The control

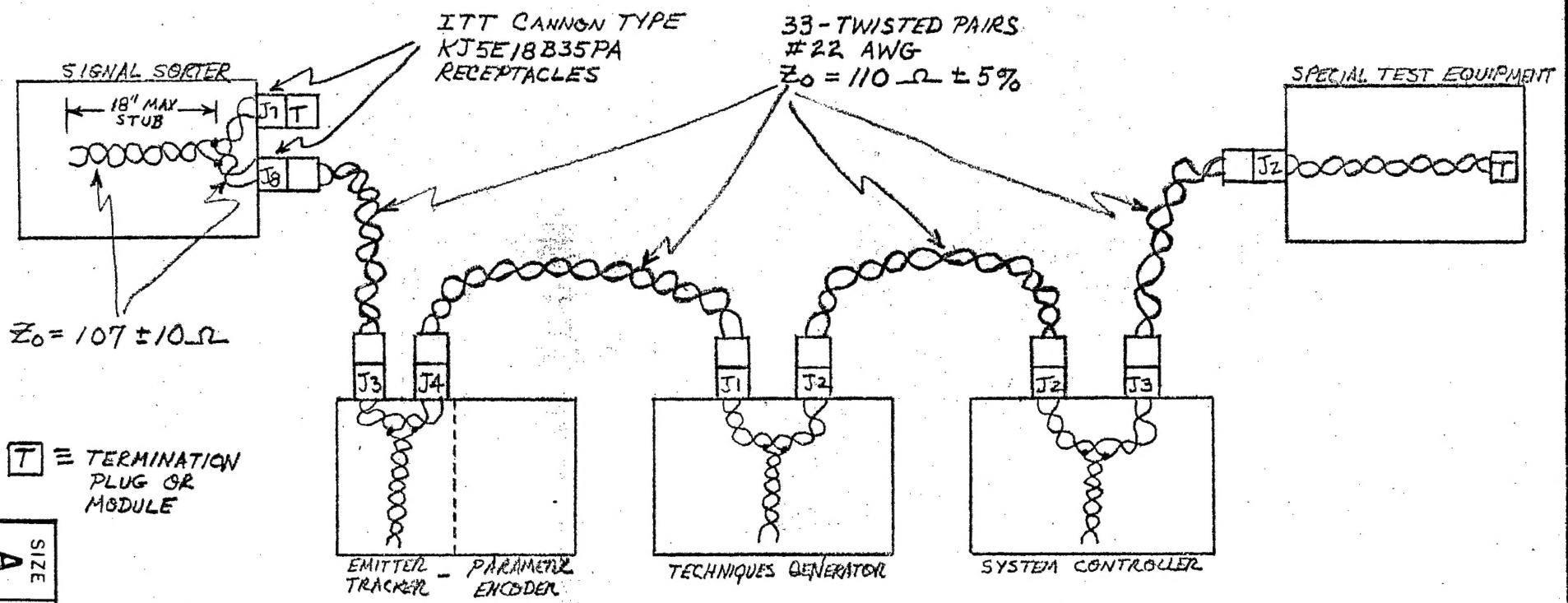

FIGURE 1. AUXILIARY BUS - SIGNAL SORTER INTERFACE

SIZE	CODE IDENT NO	DRAWING NO.
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lines shall be used to control the data transfer.

3.1.3 Bus Control

Bus control shall reside in both the Sorter and the Special Test Equipment, however, only one device shall exercise bus control at a given time. Primary control shall reside with the Sorter which shall authorize control of the bus to the Special Test Equipment.

The Sorter shall grant bus control to the Special Test Equipment by raising the ENABLE line whenever the Sorter has no output pending. The Special Test Equipment shall, respond by raising the $\overline{\text{ACTIVE}}$ line and shall assume control of the bus. The Sorter shall regain bus control by lowering the ENABLE line and the Special Test Equipment shall respond by lowering the $\overline{\text{ACTIVE}}$ line and relinquish bus control. The $\overline{\text{ACTIVE}}$ line shall not be lowered, however, until any message in process has been transmitted.

3.1.4 Selected Pulse Descriptor Words (SPDW)

SPDW's shall be defined as Pulse Descriptor Words (PDW) which have been associated with selected active track files within the Sorter for which the System Controller has requested PDW's. These messages shall consist of PDW's with a header identifying the track file it has been associated with.

3.1.5 Jammer Pulse Words (JPW)

JPW's shall be defined as messages consisting of certain PDW and track file data which shall be outputted each time PDW associations are made with selected track files specified by the System Controller. This data shall consist of the track frequency, track azimuth, last time of arrival and the track file identification.

3.1.6 Unassociated Pulse Descriptor Word (UPDW)

UPDWs shall be defined as PDWs which have not been associated with active track files within the Sorter. These messages shall consist of PDWs with a header whose track file number is invalid.

3.2 CHARACTERISTICS

3.2.1 Performance Requirements

3.2.1.1 Interface Bus Timing. The bus timing shall be as shown in Figure 2.

3.2.1.2 Interface Bus Capacity. The bus shall have a maximum transfer capacity of four million words per second.

3.2.1.3 STE Connection. The interface shall provide proper system operation with and without the STE connected to the interface. In order that the Sorter interface operate properly without the STE response on the control line, the Sorter Enable pulse shall be a ≥ 375 nanosecond pulse. The STE must respond by lowering the $\overline{\text{ACTIVE}}$ line in ≤ 550 nanoseconds.

3.2.2 Physical Requirements

TBD.

3.3 DATA FORMATS

SPDWs, UPDWs and JPDWs shall be combined into a single output message block shown in Figure 3. The identification code shall be generated by the device, Sorter or Special Test Equipment, which is transmitting the data.

3.4 DESIGN REQUIREMENTS

3.4.1 Line Drivers/Line Receivers

All line drivers and line receivers shall incorporate SN75110 and SN75107A type devices respectively. The Auxiliary Bus shall be terminated on both ends with the termination network specified in Figure 4. The optional biasing network shall be used to bias interface lines in the absence of drivers.

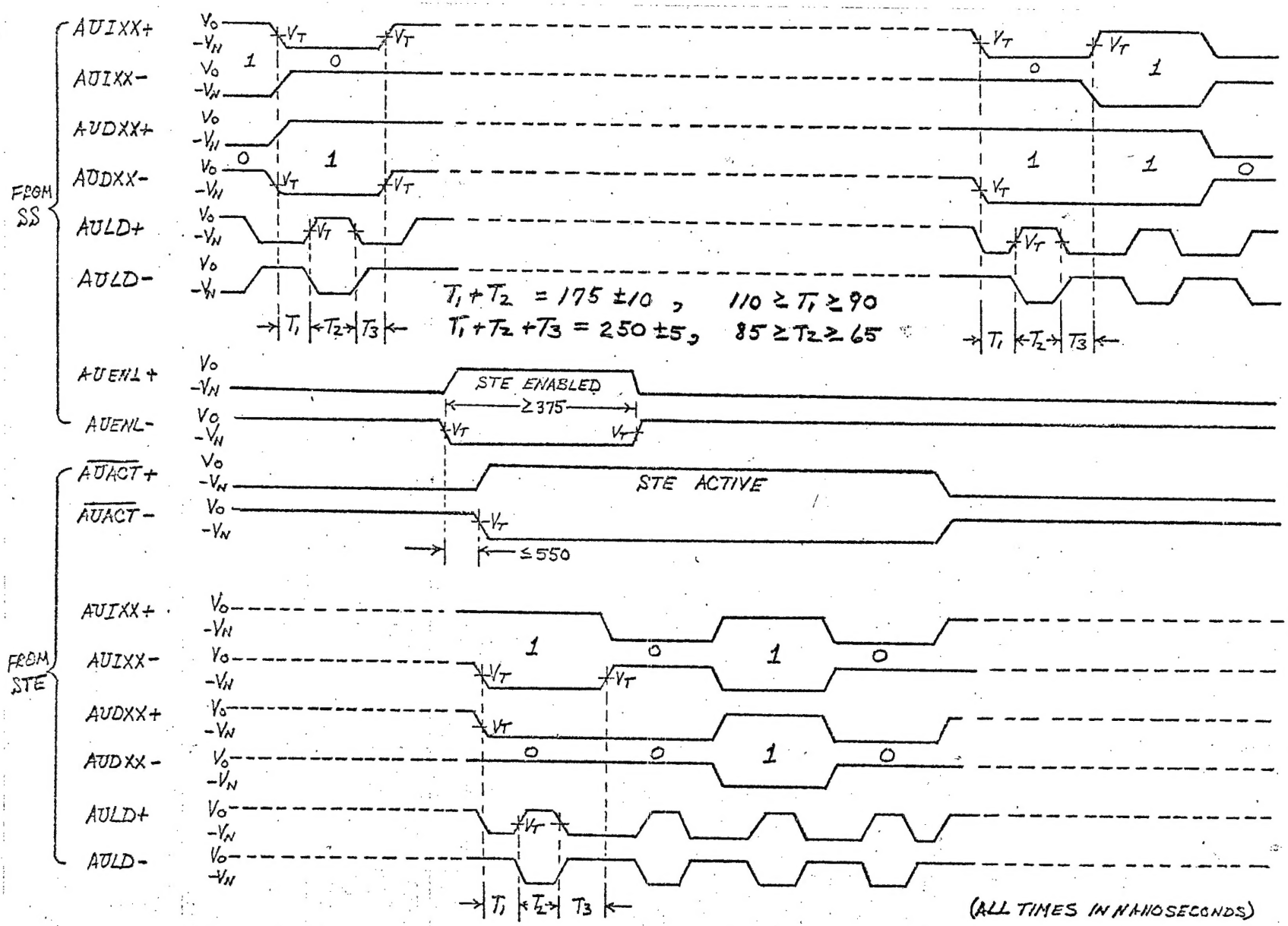

FIGURE 2. BUS TIMING

CPS 12/15/75

SIZE	CODE IDENT NO	DRAWING NO.
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3	2	1	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1

SC	AG TG	X	JAM ID				UP DW	TRK FILE ID							
FREQ														CW	MF
DATA								AZ						V	T
AMP				LI	L2	ML	TOA (MSB)					PW			
TOA (LSB)															
TRK FREQ														X	X
X	X	X	X	X	X	PRI PT	X	X	TRK AZ					X	X

FIELD	FUNCTION	BITS(S)	SIGNIFICANCE
TRK FILE ID	TRACK FILE NUMBER	0-6	—
UPDW	UNASSOCIATED PDW	7	1 = UNASSOC. PDW
JAM ID	ET CHANNEL NUMBER	8-12	TO TECH. GEN. & EMITTER TRACKER
AGTG	TECHNIQUE GEN. FLAG	14	AGTG • $\overline{\text{UPDW}}$ = TG OR ET DEST.
SC	SYSTEM CONTROLLER FLAG (CONTINUED)	15	SC V UPDW = SC DESTIN.

FIGURE 3. AUXILIARY BUS FORMAT

SIZE	CODE IDENT NO	DRAWING NO.
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FIELD	FUNCTION	BIT(S)	SIGNIFICANCE
MF	MULTIFREQUENCY INDIC.	0	1 = MULTIFREQ
CW	CW INDICATOR	1	1 = CW
FREQ.	MEASURED FREQUENCY	2-15	LSB = 1.25 MHZ
T	TEST PDW IND	0	1= TEST PDW
V	VALID	1	ALWAYS = 1
AZ	MEASURED AOA	2-7	LSB = 1 ANGLE CELL
DATA	SYSTEM CONTROLLER DATA	8-15	(SEE TABLE I)
PW	MEASURED PULSE WIDTH	0-3	(SEE TABLE II)
TOA(MSB)	MS 4 BITS OF TOA	4-7	LSB= 65,536 MICROSEC.
ML	MISSLE LAUNCH (ALR-50)	8	1 = MISSLE LAUNCH
L2	END OF LINKED PDW'S	9	1 = END
L1	LINKED PDW INDICATOR	10	1 = LINKED
AMP	MEASURED AMPLITUDE	11-15	LSB = 1.6 DBM
TOA(LSB)	LS 16 BITS OF TOA	0-15	LSB = 1.0 MICROSECOND
TRK FREQ	SMOOTHED FREQUENCY	2-15	LSB = 1.25 MHZ
TRK AZ	SMOOTHED AZIMUTH	2-7	LSB = 1 ANGLE CELL
PRI PT	PRI POINTER	10	1 = TBD, 0 = TBD

FIGURE 3 (CONTINUED). AUXILIARY BUS FORMAT

SIZE	CODE IDENT NO	DRAWING NO.
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TABLE I. DATA FIELD ENCODING

BITS							
15	14	13	12	11	10	9	8

				VF *
ACN				0 0
IB	S1	S2	S BAND	0 1
PHASE COUNT				1 0
INVALID				1 1

FIELD	FUNCTION	BITS(S)	SIGNIFICANCE
ACN	ANGLE CELL NUMBER	10-15	LSB = 1 ANGLE CELL
S BAND	SIMULT. BAND (VALID IF MF=1)	10-12	LSB = 1 IFMR BAND
S2	SPARE	13	
S1	SPARE	14	
IB	INTRA-BAND SIMUL. PULSES	15	IB = 1, SIMUL. PULSES IN SAME BAND
PHASE COUNT	PHASE REVERSAL COUNT	10-15	LSB = 1 REVERSAL

* THE VARIABLE FIELD (VF) CODE WILL BE 00 WHENEVER MF = 0 AND THE IFM RECEIVER DOES NOT DETECT A PHASE-CODED RADAR.

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TABLE II. PULSE WIDTH ENCODING

PULSE WIDTH (NS)	BITS 0	1	2	3
0 - 200	0	0	0	0
200 - 300	0	0	0	1
300 - 350	0	0	1	0
350 - 400	0	0	1	1
400 - 450	0	1	0	0
450 - 500	0	1	0	1
500 - 550	0	1	1	0
550 - 600	0	1	1	1
600 - 700	1	0	0	0
700 - 800	1	0	0	1
800 - 900	1	0	1	0
900 - 1000	1	0	1	1
1000 - 1100	1	1	0	0
1100 - 3600	1	1	0	1
> 3600	1	1	1	0
INDETERMINATE	1	1	1	1

SIZE	CODE IDENT NO	DRAWING NO.
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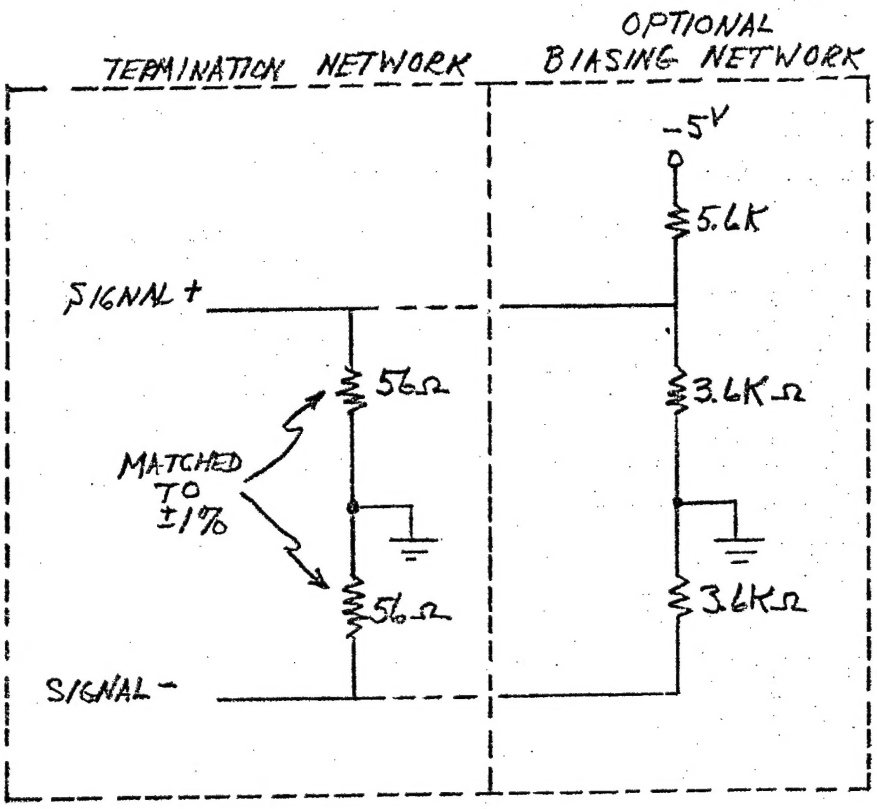

FIGURE 4. AUXILIARY BUS TERMINATION AND BIASING NETWORKS

SIZE	CODE IDENT NO	DRAWING NO.
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3.4.2 Interconnecting Transmission Lines

All interconnection cables used for this interface shall utilize twisted pair transmission line designs. The nominal impedance shall be 110 ohms ±5%.

3.4.3 Interface Signal Definition

Figure 5 gives the auxiliary bus interface signals. Signals AUD00+ and AUD00- are the signal and return respectively for the least significant data bit. AUD 15 is the most significant bit. AUI00 through AUI03 are the Identification Bits (AUI00-03 = 0000 implies message word zero). AULD is the load strobe. AUENL is the Enable Signal to the STE generated by the Sorter. $\overline{\text{AUACT}}$ originates in the STE when it assumes bus control. Pin connections for J7 and J8 shall be identical.

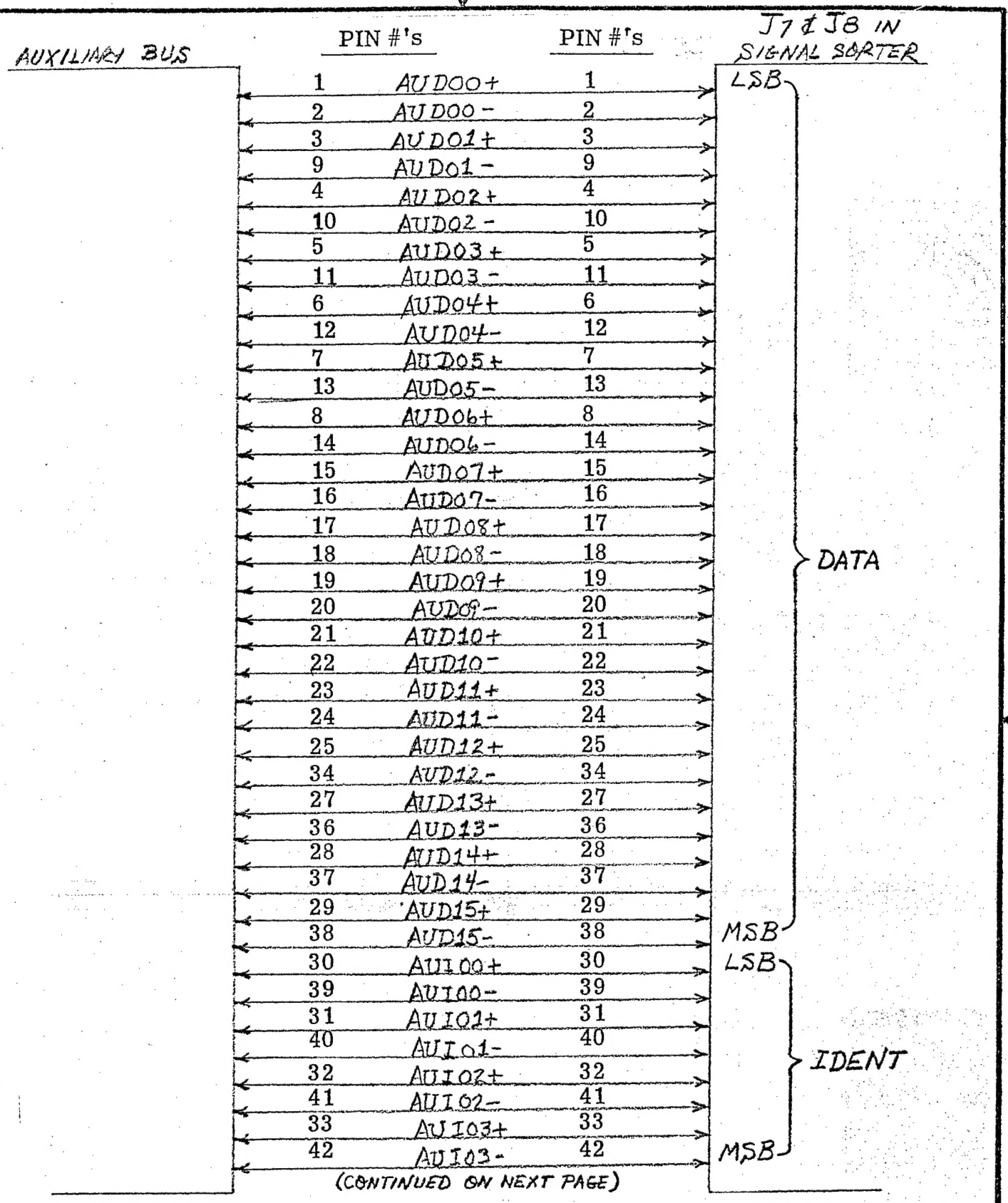

FIGURE 5. INTERFACE SIGNAL LIST

SIZE	CODE IDENT NO	DRAWING NO.
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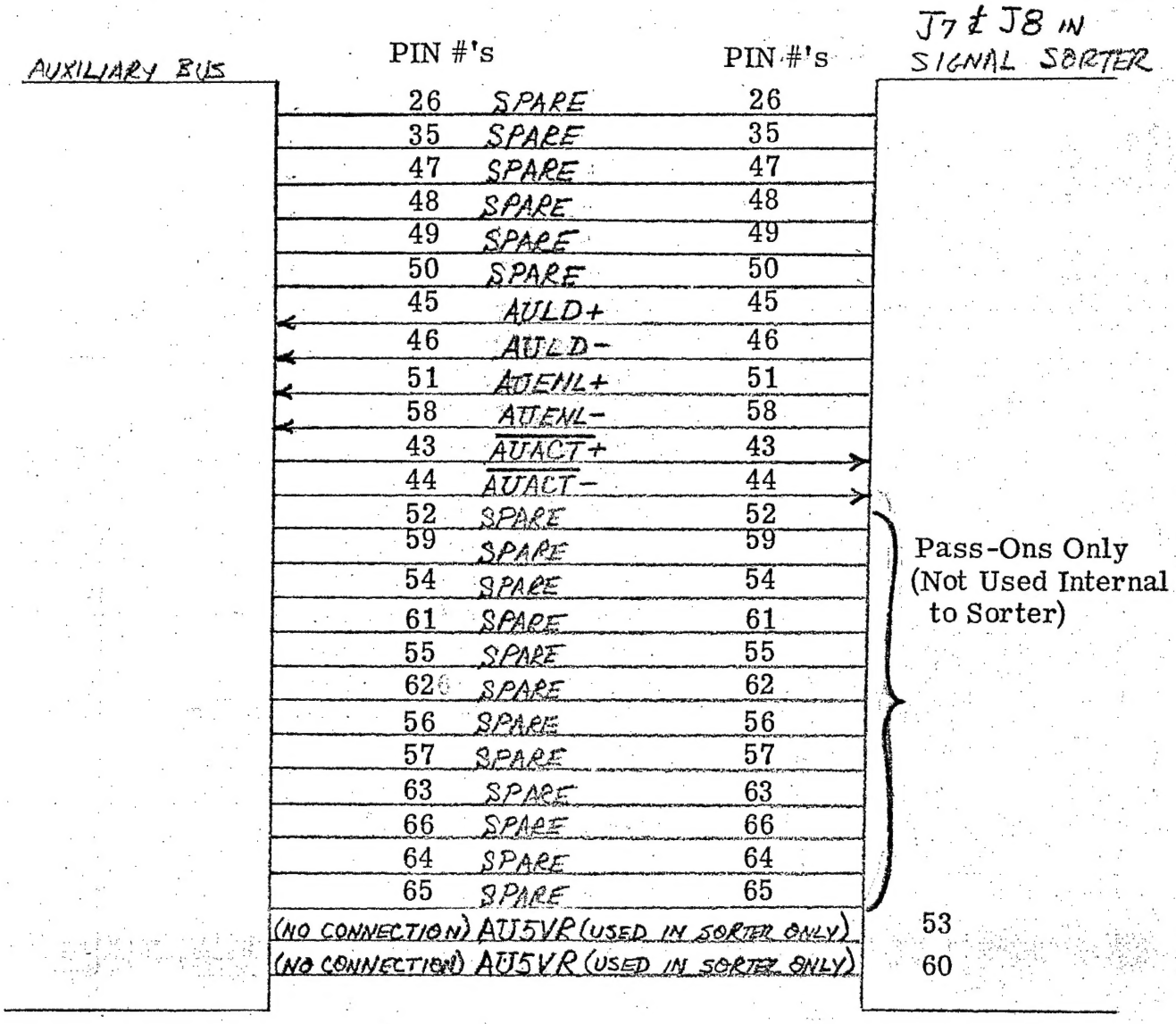

FIGURE 5. (CONT.) INTERFACE SIGNAL LIST

SIZE	CODE IDENT NO	DRAWING NO.
A	49956	53959-JK-1003
SCALE	REV 2	SHEET 14 of 14